In th Claims

CLAIMS

Claims 1-30 (Cancelled).

31. (New) Integrated circuitry comprising:

a substrate;

a plurality of spaced conductive layers over the substrate and comprising upper surfaces;

a low-K material disposed over the substrate and between the conductive layers, an entirety of the low-K material being elevationally below the upper surfaces of the conductive layers; and

a dielectric material having a first portion disposed over the low-K material elevationally below and between the upper surfaces of the conductive layers and a second portion disposed over the upper surfaces of the conductive layers.

32. (New) The circuitry of claim 31 wherein the low-K material comprises a first low-K material and wherein the dielectric material comprises a second low-K material different from the first low-K material.

33. (New) The circuitry of claim 31 wherein the dielectric material comprises a hydrogen silsesquioxane material.

34. (New) The circuitry of claim 31 wherein the low-K material comprises a carbon-comprising silicon oxide material.

35. (New) The circuitry of claim 31 wherein the low-K material comprises a first low-K material and wherein the dielectric material comprises a second low-K material having the same composition as the first low-K material.

36. (New) The circuitry of claim 31 further comprising a barrier layer disposed between the low-K material and the dielectric material.

37. (New) The circuitry of claim 31 further comprising two barrier layers disposed between the low-K material and the dielectric material.

38. (New) The circuitry of claim 31 further comprising at least two barrier layers disposed between the spaced conductive layers.

39. (New) The circuitry of claim 31 further comprising a barrier layer disposed between the upper surfaces of the spaced conductive layers and the dielectric material.

40. (New) The circuitry of claim 31 further comprising a barrier layer having a first portion disposed between the upper surfaces of the spaced conductive layers and the dielectric material and a second portion disposed between the low-K material and the dielectric material.

41. (New) Integrated circuitry comprising:

a substrate;

a plurality of spaced blocks extending upward from the substrate, the spaced blocks comprising a first portion and a second portion over the first portion, the first portion comprising a low-K material and the second portion comprising sacrificial material, and the second portion comprising an upper surface of the spaced blocks; and

a conductive material disposed between the spaced blocks, the conductive material comprising an upper surface substantially coextensive with the upper surface of the spaced blocks.

42. (New) The circuitry of claim 41 wherein the sacrificial material comprises a dielectric material other than a low-K material.

43. (New) The circuitry of claim 41 wherein the sacrificial material comprises silicon oxide material.

44. (New) The circuitry of claim 41 wherein the sacrificial material comprises oxide material.

45. (New) The circuitry of claim 41 further comprising a barrier layer disposed between the first and second portions of the spaced blocks and disposed elevationally below the upper surface of the spaced blocks.

46. (New) The circuitry of claim 41 further comprising a barrier layer disposed between the conductive material and the spaced blocks.

47. (New) The circuitry of claim 41 wherein the sacrificial material comprises a material having a dielectric constant between that of silicon dioxide and silicon nitride.

48. (New) The circuitry of claim 41 wherein the sacrificial material comprises a material having a dielectric constant greater than about 3.7 to 7.0.

49. (New) The circuitry of claim 41 further comprising a barrier layer disposed between the first and second portions of the spaced blocks, the barrier layer comprising material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, nitrogen-comprising amorphous carbon, hydrogen-comprising amorphous carbon and silicon, and nitrogen-comprising amorphous carbon.

50. (New) The circuitry of claim 41 wherein the sacrificial material comprises a thickness in the range of approximately 100 nm to approximately 1000 nm.